An Effect of Process Variation on 3T-1D DRAM

Yogesh N. Thakre, Shubhada S. Thakare, Devendra S. Chaudhari

Abstract— This paper deals with the design and analysis of 3T-1D DRAM cell to develop process variation architecture using Tanner EDA Tool. In this paper power dissipation analysis for DRAM design have been carried out for different nanotechnology with different voltages. The major contribution of power dissipation in DRAM is off –state leakage current. Thus improving the power efficiency of DRAM is critical to the overall system power dissipation. Generally process variation will greatly impact the stability, leakage power consumption and performance of future microprocessor. The absence of the capacitor is advantageous in terms of scalability, process and fabrication complexity, compatibility with the logic processing steps, device density, yield and cost. In this paper, 3T-1D DRAM cell are designed with schematic design technique of Tanner EDA Tool for the comparison of power dissipation.

Index Terms— Dynamic RAM (DRAM), Cell, Power Dissipation, 3T-1D (Three transistor- one diode), leakage, technology, etc.

1 Introduction

TECHNOLOGY nanoscaling promises increasing transistor density and increasing performance in microprocessor. In modern microprocessor on chip memory consume a significant portion of overall die space, providing high system performance in exchange for the space and power they consume. [1] As continuous technology change for high density memories favors small memory cell sizes, the dynamic RAM cell with a small structure has become a popular choice, where binary data are stored as a charge in a capacitor and the presence or absence of stored charged determine the value of stored bit. The data stored in a capacitor based DRAM cell cannot retain indefinitely, because the leakage current eventually remove or modify the stored data. Thus the capacitor based DRAM required periodic refreshing of the stored data, so that unwanted modification due to leakage is prevented before they occur. Also scaling of this capacitor is critical job; hence to avoid scaling limitation new circuit and architecture solution are needed. The problem of scaling and leakage – as well as device size – rests fundamentally with the basic transistor/capacitor building block. While the transistor element is theoretically scalable – at least for the foreseeable future – the capacitor is not. Capacitors can be fabricated as high stacks above the wafer surface or deep trenches inside the wafer to maximize the surface area and thus the capacitance per unit footprint area. However, if the overall bit cell size shrinks due to increased density or a smaller process node, then the capacitor will have to be made higher or deeper in order to maintain the minimum charge required for reliable operation. We are fast approaching the scaling limits for the capacitor element, and a new approach or a DRAM replacement will be needed. In this paper, we design on chip memory architecture based on 3T-1D dynamic memory cell without capacitor.

- ***Yogesh N. Thakre**, Department of Electronics and Telecommunication, Government College of Engineering, Amravati, India, +919975629591, (e-mail: yash4767@gmail.com).*
- ***Shubhada S. Thakare,** Department of Electronics and Telecommunication, Government College of Engineering, Amravati, India,+919637277216, (e-mail: thakare.shubhada@gcoea.ac.in).*
- ***Dr. Devendra S. Chaudhari,** Department of Electronics and Telecommunication, Government College of Engineering, Amravati, India, +919421821030, (e-mail: ddsscc@yahoo.com).*

2 Comparison Between 1T-1C and 3T-1D DRAM

Dynamic random access memory (DRAM) is a type of random access memory. DRAM cell consists of one transistor and one capacitor. Capacitor stores the information in terms of the charge and the transistor is used to write and read the stored information. Each bit of data is stored in a separate capacitor within an integrated circuit. Due to the leakage of the capacitors, the information eventually fades unless the capacitor charge is refreshed periodically. This refresh requirement makes DRAM a dynamic memory as opposed to a static memory.

2.1 Limitation of 1T-1C DRAM Cell

Dynamic random access memory (DRAM) is a type of memory that stores each bit of data in a separate capacitor within an integrated circuit. The basic DRAM cell consists of one transistor and one capacitor as shown in Fig.1. Due to the leakage of the capacitors, the information eventually fades unless the capacitor charge is refreshed periodically. This refresh requirement makes DRAM a dynamic memory as opposed to SRAM (Static random access memory).

Recently the capacitorless single-transistor (1T) DRAMs have attracted attention, due to the lack of the capacitor and the problems associated with the scaling of the capacitor, and due to its ability to achieve higher device density. The information is stored as different charge levels at a capacitor in conventional 1T/1C DRAM. The advantage of DRAM is its structural simplicity: only one transistor and a capacitor are required per bit, compared to six transistors in SRAM. This allows DRAM to reach very high density.

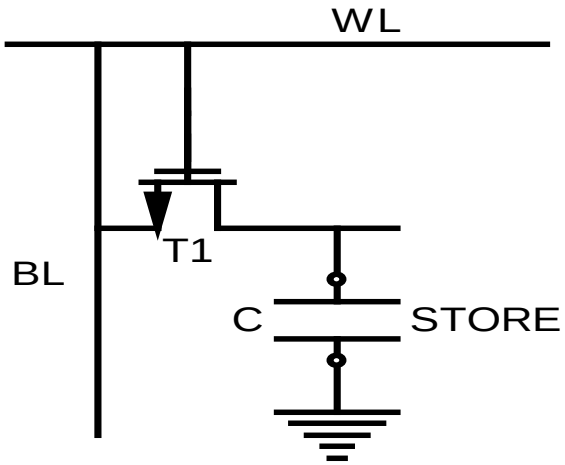

Fig.1: One transistor- one capacitor DRAM

The DRAM industry has achieved miracles packing more and more memory bits per unit area in a silicon die. But, the scaling of the conventional 1Transistor/1Capacitor (1T/1C) DRAM is becoming increasingly difficult, in particular due to the capacitor which has become harder to scale, as device geometries shrink. Apart from the problems associated with the scaling of the capacitor, scaling introduces yet another major problem for the DRAM manufacturers which is the leakage current. In both the memory cell as well as the supporting circuitry, leakage becomes more significant as complementary metal-oxide-semiconductor (CMOS) processing nodes progress from different nanotechnology. However, if the overall bit cell size shrinks due to increased density or a smaller process node, then the capacitor will have to be made higher or deeper in order to maintain the minimum charge required for reliable operation. We are fast approaching the scaling limits for the capacitor element, and a new approach or a DRAM replacement will be needed. This replacement is possible with the help 3T-1D structure. In this 3T-1D DRAM structure by simply joining source and drain of N-mos transistor we can produce voltage controlled capacitor diode hence give the name 3T-1D cell.

2.2 Introduction to 3T-1D DRAM Cell

A Memory architecture using three-transistor, one-diode DRAM (3T1D) cell is given below in which capacitor get replace by diode D which acts as voltage controlled capacitor. Figure 3(a) presents a schematic of the 3T1D (3-transistor, 1-diode) DRAM cell.

Due to the threshold voltage of T1, there is a degraded level on the storage node when storing a "1". Hence, it relies on a "gated diode" (D1) to improve array access speed. This diode can be thought of as being a voltage-controlled capacitor with larger capacitance when storing a "1" and a smaller capacitance when storing a "0." Each time the cell is read, the bottom side of this capacitor is also raised to VDD. If the cell stores a "1" and it is read, the charge stored on the big capacitor of D1 boosts up the turn-on voltage of T2, rapidly discharging the bitline. As a result, the access speed can match the speed of 6T SRAM cells. Conversely, when a "0" is stored, the capacitance of D1 is smaller and there is almost no voltage boosting, which keeps T2 off during the read. Hspice simulation results, shown in Figure 2, illustrate the operation of the 3T1D cell. The gate voltage of T2 is boosted by about 1.5-2.5 times (1.13V) the originally stored voltage (0.6V) if a "1" is stored when being read. Although the speed of a 3T1D cell can be fast, this high-speed access is only valid for a limited time period after each write to the cell. This is because the charge on D1 leaks away over time. With this stored charge leaking away, the access time increases until finally it exceeds the array access time of the 6T SRAM cell. Traditionally, the word "retention time" is defined as the time a DRAM cell can no longer hold the stored value.

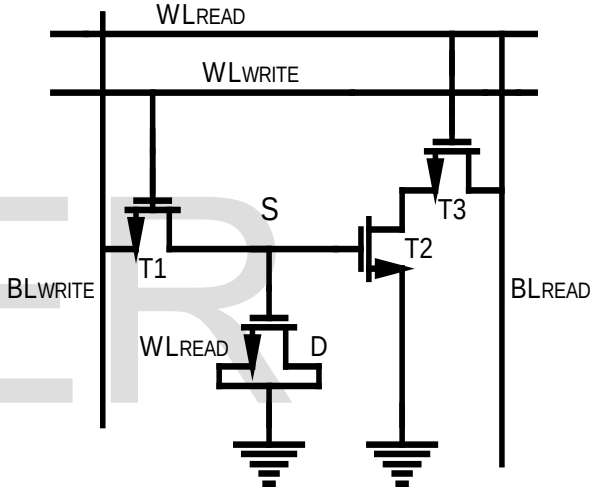

Fig.2: Three Transistor –One Diode DRAM

3 Experimental Methodology In Tanner Tool

In this we are implementing one by one conceptual architectural component required for design of DRAM using Tanner EDA tool. The design flow chart is shown below;

Desig step of architecture in Tanner EDA tool;
Step 1:- Open S-edit.
Step 2:- Create a schematic view.
Step 3:- Generate symbol of design.
Step 4:- Built a desig using symbolic view.
Step 5:- Check for errors in T-spice.
Step 6:- If simulation is successful then check the output waveform in W-edit.
Step 7:- Save the design.

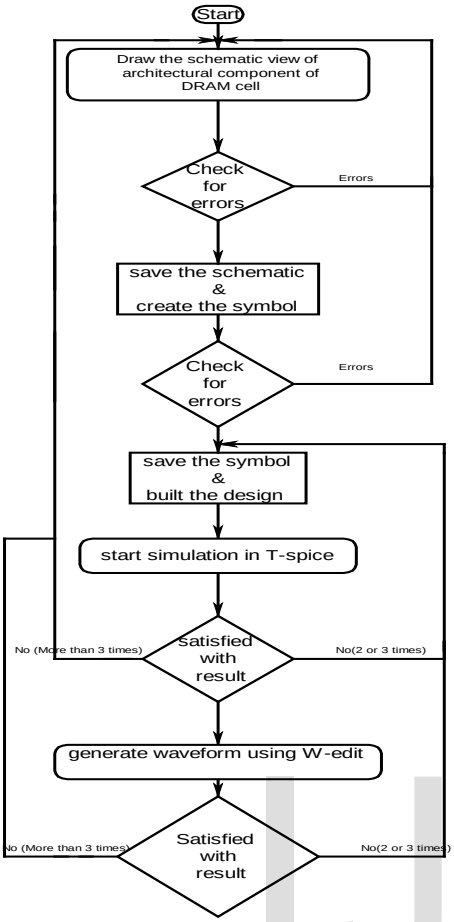

Fig. 3: Three Transistor –One Diode Dram

3.1 Proposed 3T-1D System Architecture Model

In light of such problems with the standard 6T SRAM design, researchers are investigating new cell designs that can better withstand process variation. 3T1D cell is one of the possible options proposed by Luk et al. [4]. 3T1D is a DRAM memory cell that, unlike a typical 1T or 1T1C design, provides non-destructive reads and high-speed operation that is comparable to (and in some cases better than) the standard 6T SRAM cell. 3T1D is also more compact and dissipates less leakage power than the 6T cell [1]. Moreover, it does not suffer from the stability issues that are present in the 6T design: its operation does not rely on the specific device balance, and device mismatch is less likely to cause failure within the cell. Variation only affects the operating frequency of the cell, making it much more robust to process variation than the 6T design. Figure 4 presents a schematic of a 3T1D cell.

3.1.1 Schematic of 3T-1D Cell

The schematic view of 3T-1D cell in 1µm technology is shown below. To write to the cell, the write bitline is charged to the value we wish to store in the cell, and the write wordline is strobe. To write to the cell, the write bitline is charged to the value we wish to store in the cell, and the write wordline is strobe. To read from the cell, the read bitline is precharged high and the read wordline is strobe. To write to the cell, the write bitline is charged to the value we wish to store in the cell, and the write wordline is strobe. To read from the cell, the read bitline is precharged high and the read wordline is strobe. If a 1 is stored in the cell, transistor T2 turns on and the bitline discharges. The key to fast access times is the gated diode, which is tied to the read wordline. When a 1 is stored in the cell, the diode provides a "boosting" effect to the value at the storage node and temporarily gives it a value close to (and sometimes greater than) Vdd, which allows T2 to turn on quickly and discharge the bitline.

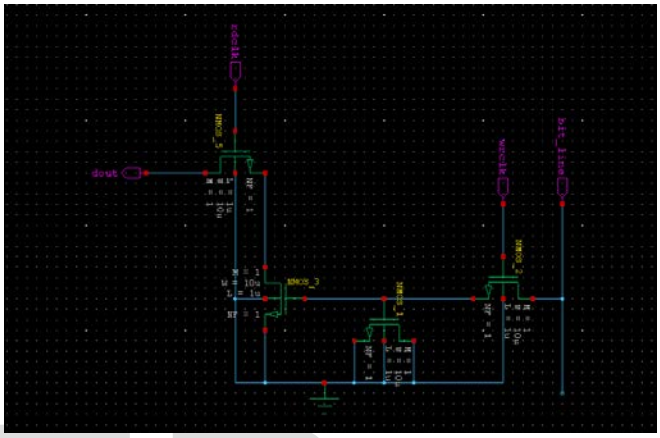

Fig. 4: Schematic of 3Transistor 1 Diode DRAM cell

When a 0 is stored in the cell, the capacitance of D1 is smaller and little to no voltage boosting occurs, keeping T2 turned off. Because the 3T1D is a dynamic memory cell, the value at the storage node leaks away as time passes. As this happens, accesses to the cell become slower and slower. Eventually, this access time becomes so slow that it is no longer comparable to that of the 6T cell. Eventually, the stored value degrades completely. While the fast access times and non-destructive reads of the 3T1D cell produce an attractive 6T cell alternative, 3T1D's dynamic nature introduces a new issue that SRAM designers need not consider. The input and output of 3T-1D DRAM cell in 1µm Tanner technology is shown below.

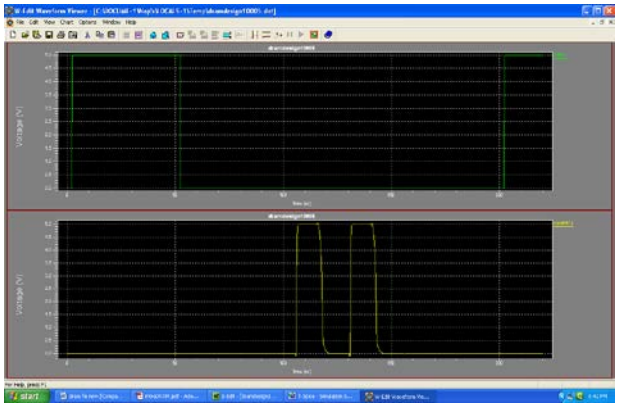

Fig.5: Input/output waveform of 3T-1D DRAM Cell

3.1.2 Schematic of 3T-1D DRAM Cache Architecture

Dynamic random access memory (DRAM) integrated circuits (ICs) have existed for more than twenty-five years. DRAMs evolved from the earliest 1-kilobit (Kb) generation to the recent 1-gigabit (Gb) generation through advances in both semiconductor process and circuit design technology. Tremendous advances in process technology have dramatically reduced feature size, permitting ever higher levels of integration. These increases in integration have been accompanied by major improvements in component yield to ensure that overall process solutions remain cost-effective and competitive. Technology improvements, however, are not limited to semiconductor processing. Many of the advances in process technology have been accompanied or enabled by advances in circuit design technology. In this chapter, we introduce some fundamentals of the DRAM IC, assuming that the reader has a basic background in complementary metal-oxide semiconductor (CMOS) circuit design, layout, and simulation.

In this project we try to design 16-bit DRAM (16 x 1 bit). Schematic diagrams of 3T-1D DRAM cache architecture is shown below. Note that there are 4 address inputs with pin labels *R1-R2* and *C1-C2.* Each address input is connected to an on-chip address input buffer. The input buffers that drive the row *(R)* and column *(C)* decoders in the schematic diagram have two purposes; to provide a known input capacitance *(CM)* on the address input pins and to detect the input address signal at a known level so as to reduce timing errors. The level *VTRIP*> an idealized trip point around which the input buffers slice the input signals, is important due to the finite transition times on the chip inputs (Figure 6). Ideally, to avoid distorting the duration of the logic zeros and ones, *VTRIP* should be positioned at a known level relative to the maximum and minimum input signal amplitudes. In other words, the reference level should change with changes in temperature, process conditions, input maximum amplitude *(Vm),* and input minimum amplitude *(VIL).* Having said this, we note that the input buffers used in first-generation DRAMs were simply inverters. Continuing our discussion of the block diagram shown in Figure 6, we see that five address inputs are connected through a decoder to the 16-bit memory array in both the row and column directions. The total number of addresses in each direction, resulting from decoding the2-bit word, is 4. The single memory array is made up of 16 memory elements laid out in a square of 4 rows and 4 columns. Figure 6 illustrates the schematic view of this memory array. A memory element is located at the intersection of a row and a column.

By applying an address of all zeros to the 4 address input pins, the memory data located at the intersection of row 0, *RAO,* and column 0, *CAO,* is accessed. (It is either written to or read out, depending on the state of the *R/W* input and assuming that the CE pin is LOW so that the chip is enabled.) It is important to realize that a single bit of memory is accessed by using both a row and a column address. Modern DRAM chips reduce the number of external pins required for the memory address by using the same pins for both the row and column address inputs *(*address multiplexing*).* A clock signal row address strobe *(RAS)* strobes in a row address and then, on the same set of address pins, a clock signal column address strobe *(CAS)* strobes in a column address at a different time.

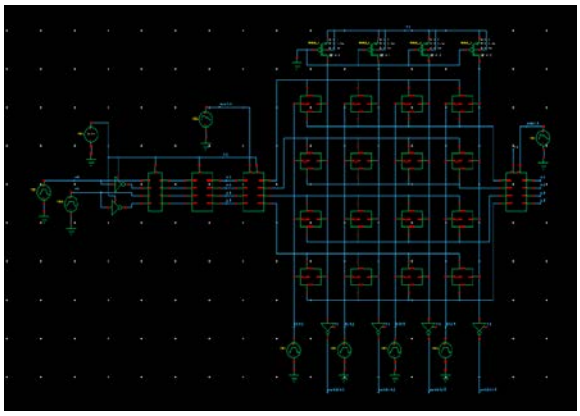

Fig. 6: Schematic of 3Transistor 1 Diode DRAM cell

Also note how a first-generation memory array is organized as a logical square of memory elements. At this point, we don't know what or how the memory elements are made. We just know that there is a circuit at the intersection of a row and column that stores a single bit of data. The input and output waveform of 3T-1D DRAM cache architecture in 1µm Tanner technology is shown below.

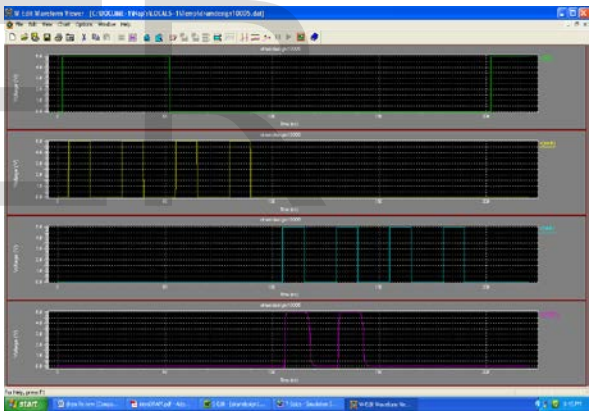

Fig.7: Input/output waveform of 3T-1D DRAM Cache

4 Simulation And Performance

As continuous technology change for high density memories favors small memory cell sizes, the dynamic RAM cell with a small structure has become a popular choice, where binary data are stored as a charge in a capacitor and the presence or absence of stored charged determine the value of stored bit. The data stored in a capacitor based DRAM cell cannot retain indefinitely, because the leakage current eventually remove or modify the stored data.

We have performed simulations using Tanner EDA tool using two methods. The main purpose of Technology variation is to determine the efficiency, power dissipation and leakage current of 3T1D DRAM Cells.

4.1 Technology Variation

In this second method voltage is kept constant and technology get changes for same DRAM architecture. The following configuration 1µm, 0.5µm, 0.35µm, 0.25µm & 0.18µm of DRAM cells were designed and analyzed using the Tanner tool. The various configurations were simulated using T-spice.

4.1.1 Voltage 5V

When applying voltage is kept constant i.e. 5V and technology changes from 1µm to 0.18µm for same 3T- 1D DRAM architecture then we get leakage current which is also called as static current (steady current). Static current is the current that flows between the supply rails in the absence of switching activity.

Table 4.1 Technology Vs Power at 5V

Technology (µm)	Static Current (A)	Power Dissipation (mW)
0.18	0.002	10
0.25	0.0018	9
0.35	0.0012	6
0.5	8.85×10^{-4}	9
1	6.54×10^{-4}	3.27

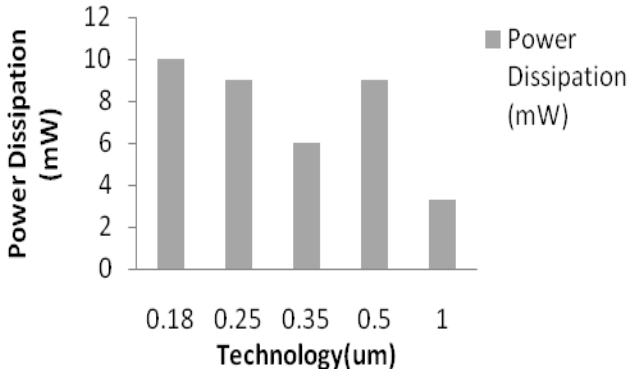

Fig. 8: Technology Vs Power at 5V

According to above graph we can conclude that when applying voltage is 5v at that time 1µm technology is best technology because it gives least power dissipation as compared to other. Also when applying voltage is 5V to 3T-1D DRAM 180nm technology gives maximum power dissipation.

4.2 Voltage Variation

In this case technology is kept constant in sub threshold region; with input voltage ranges from 5V, 4V, 3V, 2.5V and 1.8V. To establish an impartial testing environment both circuits have been tested on the same input patterns which covers all the combination of input stream.

4.2.1 Technology 1 µm

Table 4.6 Voltage Vs Power at 1µm

Voltage (V)	Power Dissipation (mW)
1.8	0.2043
2.5	0.536
[illegible]	[illegible]
[illegible]	[illegible]
[illegible]	[illegible]

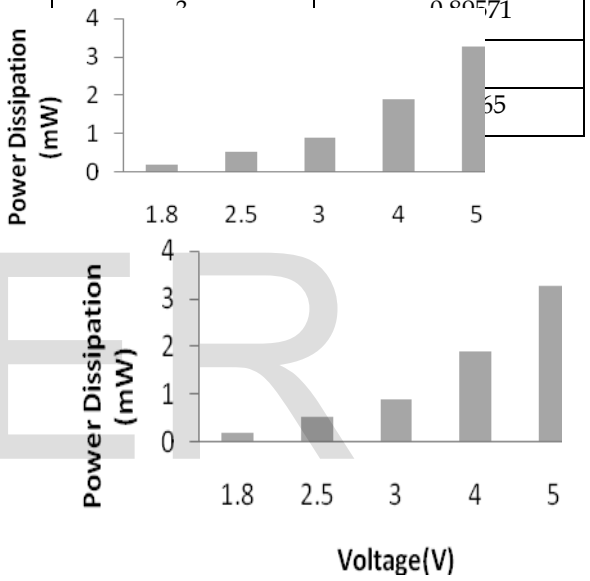

Fig. 9: Voltage Vs Power at 1µm

According to above graph we can conclude that when technology is kept constant at 1µm and applying voltages are 5V, 4V, 3V, 2.5V and 1.8V to 3T-1D DRAM it is observed that 1.8V gives least power dissipation and 5V gives maximum.

5 Conclusion

This paper proposes novel process variation in nanotechnology. Scaling of capacitor in DRAM is critical job. So it can be avoided by capacitorless DRAM out of which 3T-1D is more preferable as compare to 2T-1D DRAM cell. Hence this project proposes to replace on-chip SRAM with 3T-1D DRAM memories, with the specific target of combating process variation. With the help of this project it will possible to get high stability, reduce power requirement and the ability to tolerate performance variation. This approach provides a comprehensive solution to many of the issues that will impact on-chip memory design in nanoscale process technologies. This project proposes novel process variation tolerant on-chip memory

architectures based on a 3T-1D dynamic memory cell. The 3T-1D DRAM cell is an attractive alternative to conventional 6T cells for next-generation on-chip memory designs since they offer better tolerance to process variations that impact performance, cell stability, and leakage power.

REFERENCES

[1] X. Liang, R. Canal, G. Wei, and D. Brooks "*Replacing 6T SRAMs with 3T1D DRAMs in the L1 data cache to combat process variability*", IEEE Computer Society, Vol.8, No.1:pp.60-68, January-February 2008 .

[2] B. Raj, A. Suman & G. Singh "*Analysis of Power Dissipation in DRAM Cells Design for Nanoscale Memories*" International Journal of Information Technology and Knowledge Management, Vol. 2, No. 2, pp. 371-374 July-December 2009

[3] M. Tien Chang, P. Tsang Huang and W. Hwang "*A 65nm Low Power 2T1D Embedded DRAM with Leakage Current Reduction*" in 39th IEEE National Science Council and Ministry of Economic Affairs International Symposium on Micro architecture, Vol.1, No.12, pp.56-62, July-December 2006.

[4] S. Lin, Y. Kim and F. Lombardi "*A 32nm SRAM Design for Low Power and High Stability*" IEEE Journal of in Solid-State Circuits, Vo. 42, No. 3, pp. 680 - 688, January-March 2007.

[5] B. Amelifard, F. Fallah "*Leakage Minimization of SRAM Cells in a Dual-Vt and Dual-Tox Technology*" IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 16, No. 7, Jun-July 2008.

[6] N. Bhat " *Design and Modeling of Different SRAM's Based on CNTFET 32nm Technology*" International Journal of VLSI design & Communication Systems, Vol.3, No.1, November-February 2012.

[7] J. Koob, S. Ung, B. Cockburn, D. Elliott "*Design and Characterization of a Multilevel DRAM* " IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 19, No. 9, July- September 2011.

[8] B. Davis "*Modern DRAM Architectures*" In Proc. 26th Annual International Symposium on Computer Architecture, Vol.2, No. 26, pp. 222–233, July- December 1999.

[9] X. Liang, R. Canal, G. Wei and D. Brooks "*Process Variation Tolerant 3T1D-Based Cache Architectures*" School of Engineering and Applied Sciences, Harvard University, Cambridge, vol. 36, no. 4, pp. 658–665, 2001.

[10] S. M. Kang & Y. Leblebici "CMOS Digital Integrated Circuits Analysis and Design" 3rd edition TATA McGraw Hill Edition, pp.405-474

ABOUT AUTHOR'S

Yogesh Thakre[1] received the bachelor's degree in Electronics and Telecommunication engineering from HVPM College of Engineering & Technology, Amravati, Maharashtra, India and currently pursuing M. Tech in Electronic System and Communication from Govt. College of Engineering, Amravati, Maharashtra, India.

Shubhada Thakare[2] received the bachelor's and master's degree from Amravati University. Currently she is an Assistant Professor at Government College of Engineering, Amravati, Maharashtra, India with over 14 years of experience in teaching field. Her current areas of research are VLSI and Embedded Systems.

Devendra Chaudhari[3] obtained BE, ME, from Marathwada University, Aurangabad and PhD from Indian Institute of Technology, Bombay, Mumbai. He has been engaged in teaching, research for period of about 26 years. Presently he is working as Head, Department of Electronics and Telecommunication Engineering at Government College of Engineering, Amravati. Dr. Chaudhari published research papers and presented papers in international conferences abroad at Seattle, USA and Austria, Europe. His present research and teaching interests are in the field of Biomedical Engineering, Digital Signal Processing and Analogue Integrated Circuits.